WHAT IS CLAIMED:

1. A debug subsystem for testing a system-on-a-chip including an embedded processor and memory comprising:

at least one sub-block operable to:

monitor a bus between the processor and the memory to detect selected triggering events;

count the number of triggering events detected; and

when the number of triggering events reaches a predetermined threshold, generating a debugging signal.

2. The debug subsystem of Claim 1 wherein the triggering events comprise memory accesses.

3. The debug subsystem of Claim 2 wherein the memory accesses are selected from the group including reads and writes.

4. The debug subsystem of Claim 2 wherein the triggering events comprise memory accesses within a selected address range.

5. The debug subsystem of Claim 1 wherein the debugging signal is operable to freeze a clock timing the operation of the processor.

6. The debug subsystem of Claim 1 wherein the debugging signal comprises an interrupt to the processor.

7. The debug subsystem of Claim 1 wherein the triggering events comprise predetermined data values appearing on a data bus.

8. A system on a chip comprising:

at least one processor;

a plurality of memory spaces accessible by said processor via address and data buses; and

a debug block comprising a plurality of independently programmable debug sub-blocks each for monitoring accesses to selected one of said memories and detecting triggering events, each sub-block comprising:

a first register for setting triggering event parameters;

a second register for setting a threshold number of triggering events;

a counter for maintaining a count of detected triggering events; and

circuitry for generating a control signal when the count reaches the threshold.

9. The system of Claim 8 wherein said triggering event parameters set in said first register select the selected one of the memories, select a memory access type and select an address range for detecting the access.

10. The system of Claim 8 wherein said triggering event parameters set in said first register select a value of data accessed from the selected one of the memories.

11. The system of Claim 9 wherein said control signal freezes a clock driving said processor.

12. The system of Claim 8 wherein said control signal comprises an interrupt to said processor.

13. The system of Claim 8 further comprising a second processor and said control signal comprises an interrupt to at least one of said processors.

14. The system of Claim 8 wherein said second processor can access said memories and generate trigger events.

15. The system of Claim 8 wherein said processor comprises a digital signal processor and said second processor comprises a microprocessor.

16. A method of debugging a single-chip system including an embedded processor and memory comprising the steps of:

selecting triggering event parameters;

monitoring transactions between the processor and the memory to detect triggering events corresponding to the selected triggering parameters;

counting the number of triggering events detected; and

when the number of triggering events reaches a predetermined threshold, generating a debugging signal.

17. The method of Claim 16 wherein said step of selecting triggering event parameters comprises the substeps of:

selecting a triggering memory access type; and

selecting a triggering address range.

18. The method of Claim 16 wherein the memory comprises a plurality of memory spaces and said step of selecting triggering event parameters comprises the step of selecting one of the memory spaces for monitoring.

19. The method of Claim 16 wherein said step of monitoring comprises the step of monitoring an address bus to the memory for memory accesses meeting the triggering event parameters.

20. The method of Claim 16 wherein said step of selecting triggering event parameters comprises the step of selecting triggering events to step through code being run by the processor.